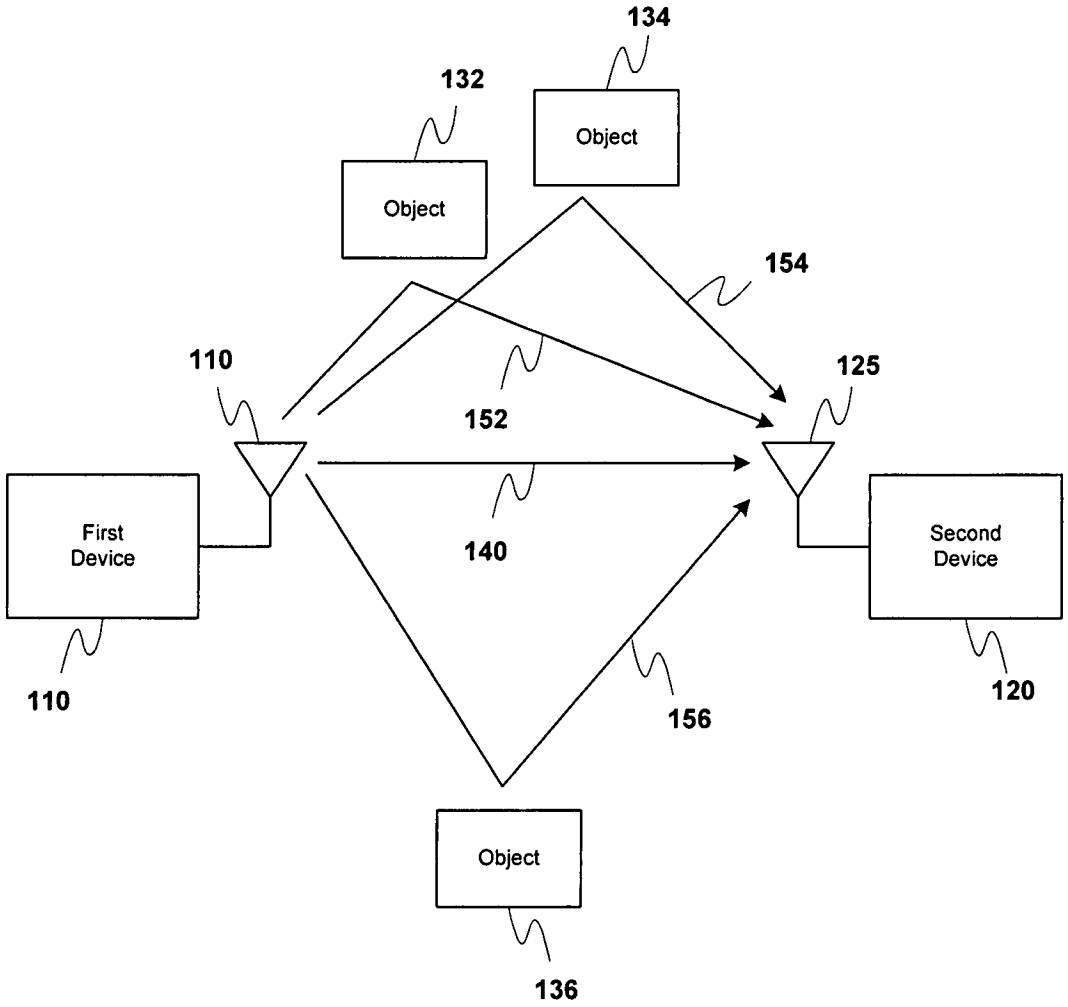
134
132
Object
Object
154
110
152
125
First
Device
140
Second
Device
110
156
120
Object
136

Fig. 1

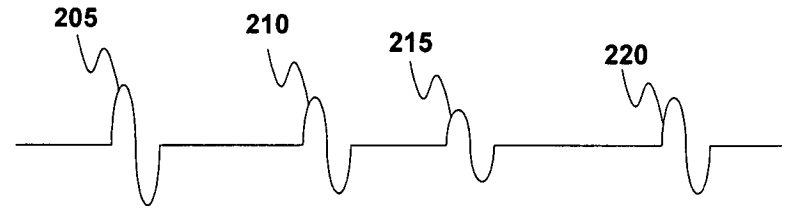

Fig. 2A

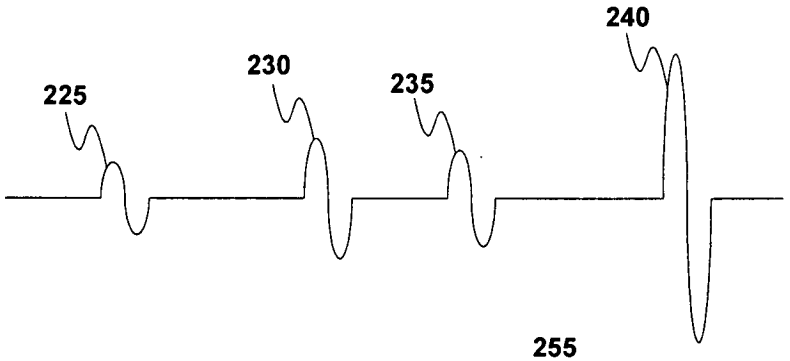

Fig. 2B

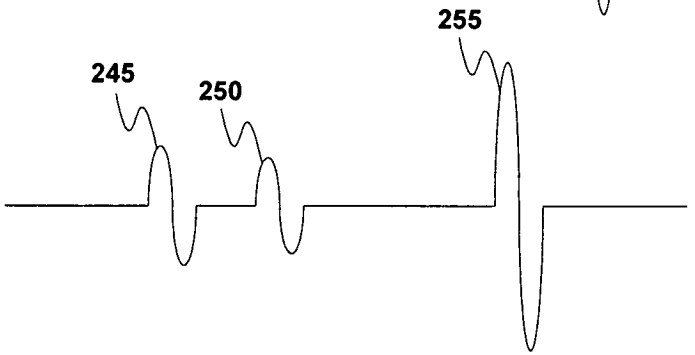

Fig. 2C

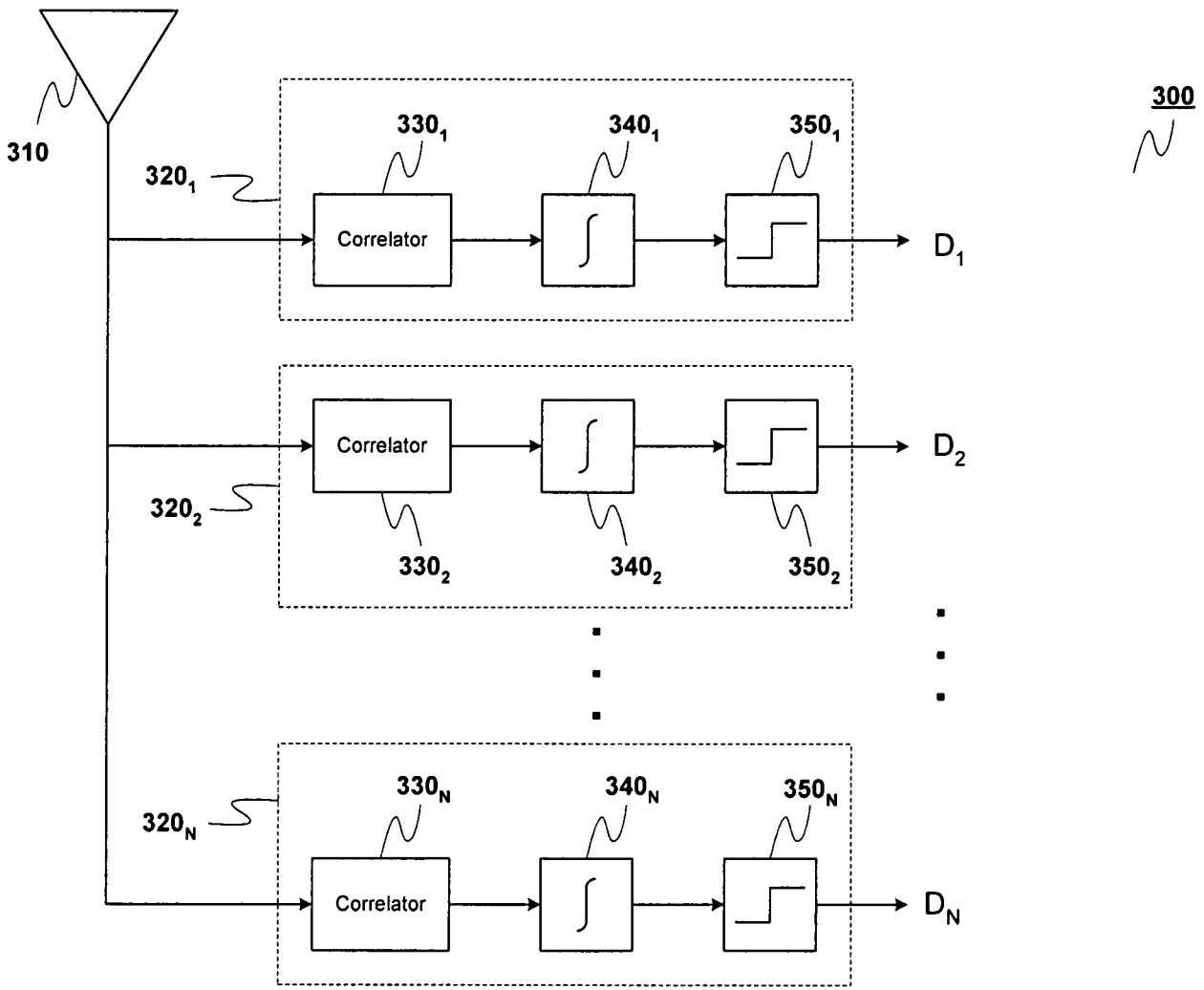
300
310
320$_1$
330$_1$
340$_1$
350$_1$
Correlator
D_1
320$_2$
330$_2$
340$_2$
350$_2$
Correlator
D_2
320$_N$
330$_N$
340$_N$
350$_N$
Correlator
D_N

Fig. 3

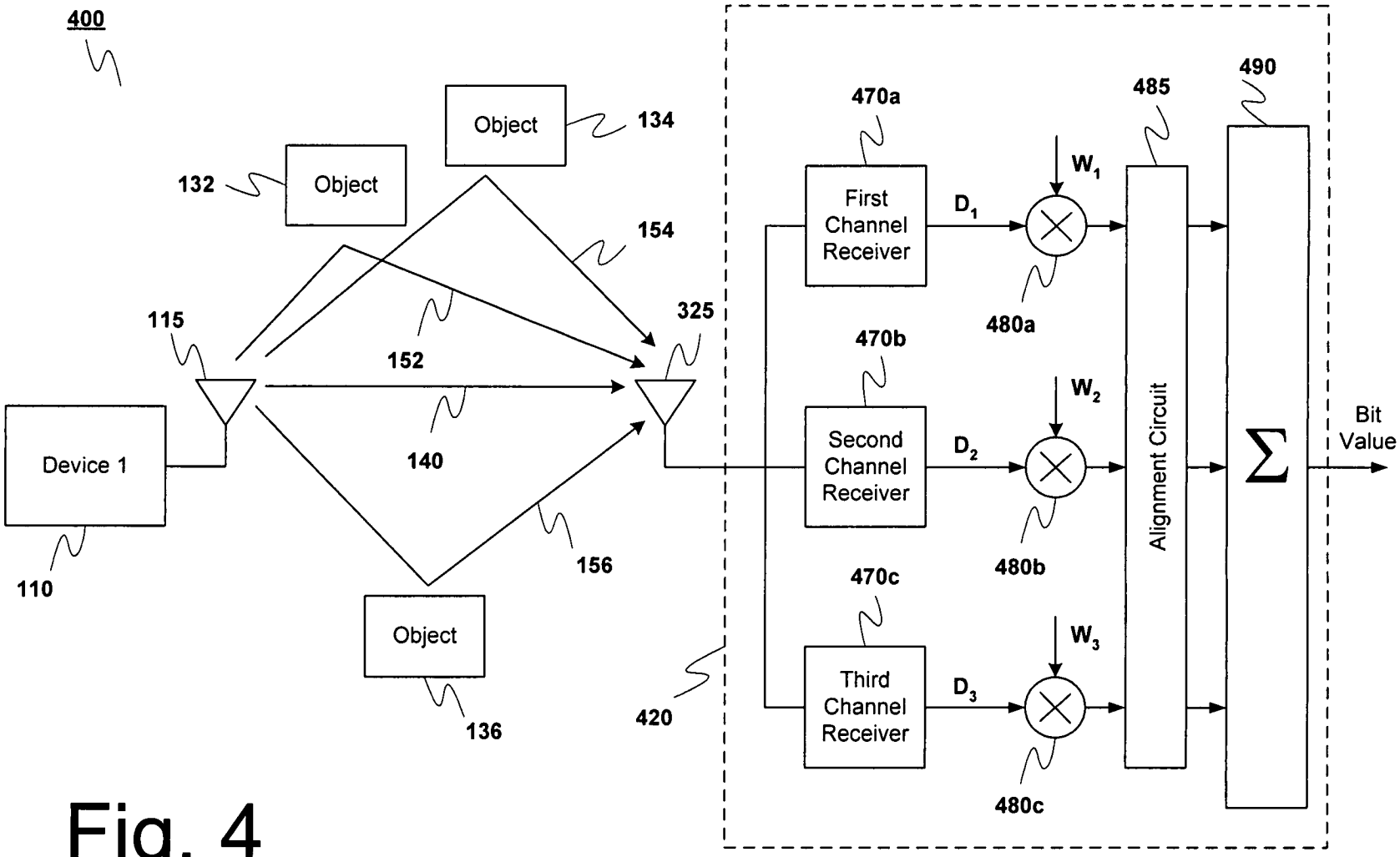
400
Object
134
Object
132
154
152
115
325
140
Device 1
110
156
Object
136
420
470a
First Channel Receiver
D1
W1
480a
485
490
470b
Second Channel Receiver
D2
W2
480b
Alignment Circuit
Σ
Bit Value
470c
Third Channel Receiver
D3
W3
480c

Fig. 4

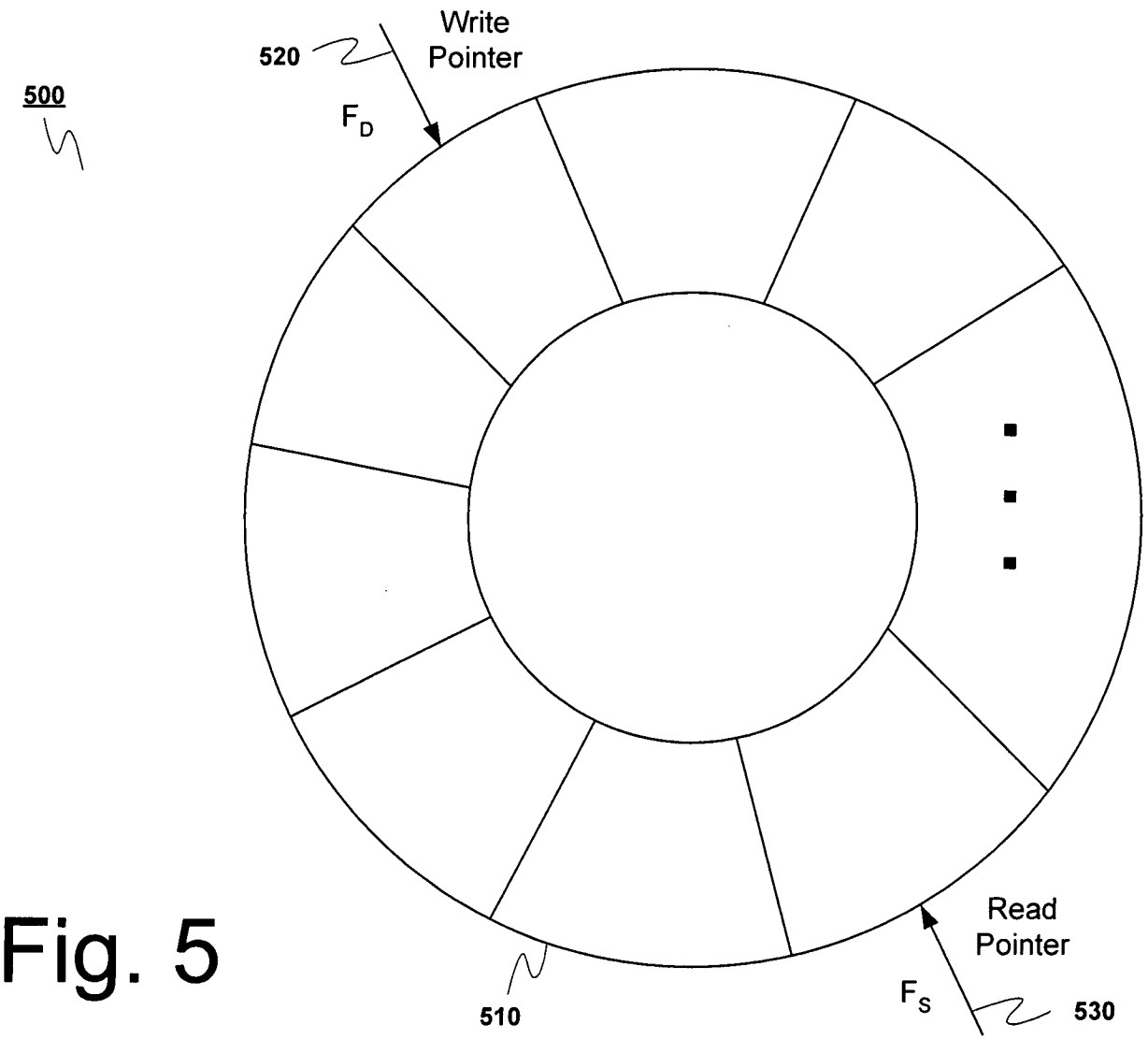

Fig. 5

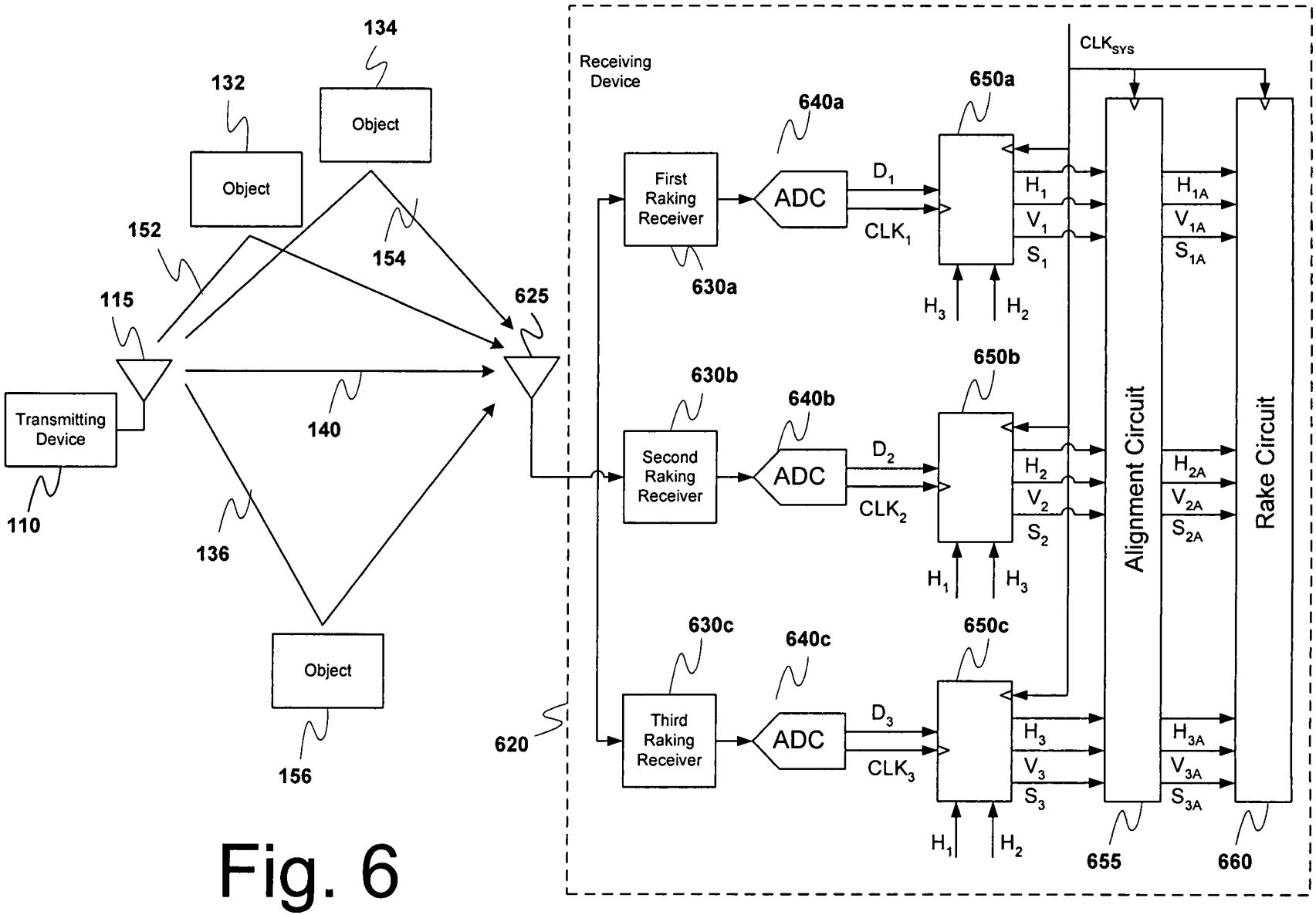
134
132
Object
Object
152
154
115
625
Transmitting Device
140
110
136
Object
156
620
Receiving Device
640a
650a
First Raking Receiver
ADC
D1
CLK1
630a
H3
H2
CLKSYS
H1
V1
S1
H1A
V1A
S1A
630b
640b
650b
Second Raking Receiver
ADC
D2
CLK2
H1
H3
H2
V2
S2
H2A
V2A
S2A
630c
640c
650c
Third Raking Receiver
ADC
D3
CLK3
H1
H2
H3
V3
S3
H3A
V3A
S3A
Alignment Circuit
Rake Circuit
655
660

Fig. 6

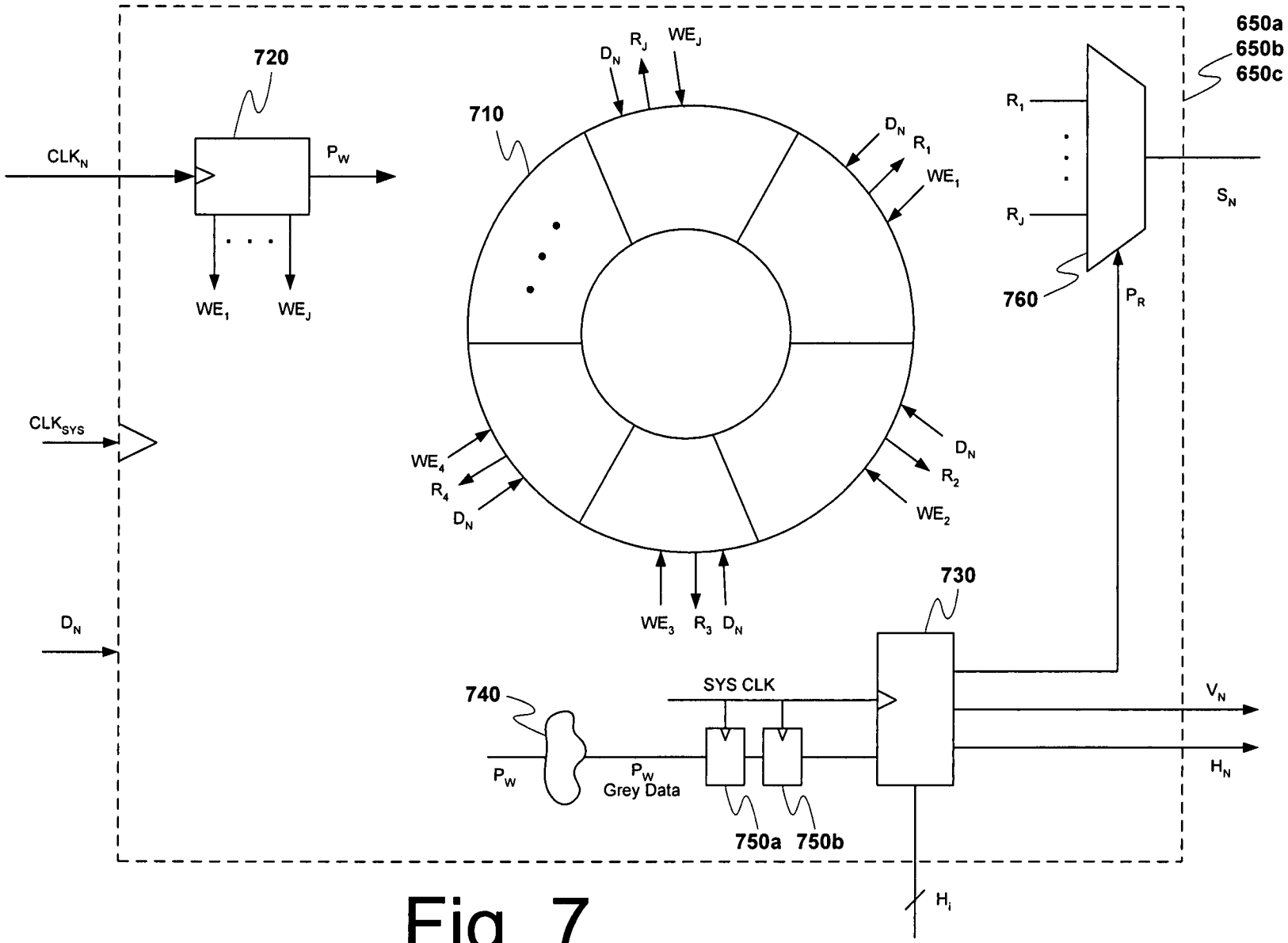
720
CLK_N
P_W
WE_1
WE_J
710
D_N
R_J
WE_J
D_N
R_1
WE_1
WE_4
R_4
D_N
D_N
R_2
WE_2
WE_3
R_3
D_N
650a
650b
650c
R_1
R_J
S_N
760
P_R
CLK_SYS
D_N
730
740
P_W
P_W
Grey Data
SYS CLK
750a
750b
V_N
H_N
H_i

Fig. 7

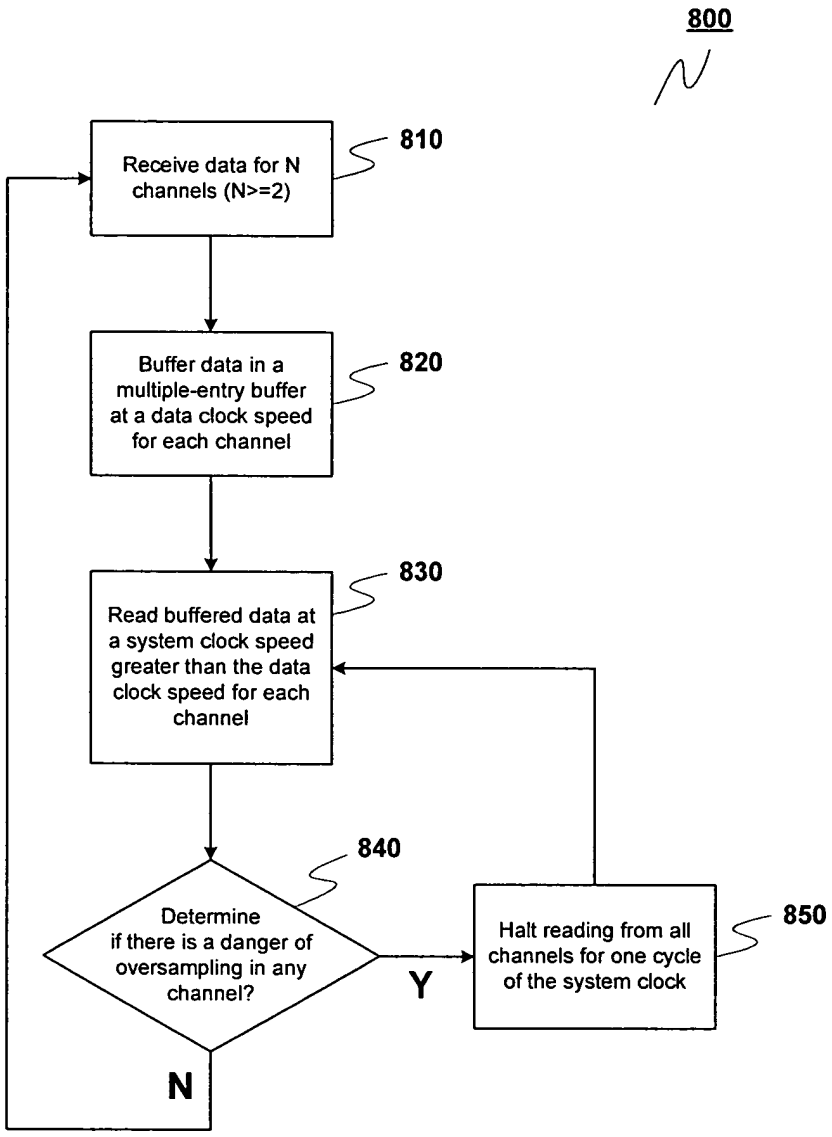
800
Receive data for N channels (N>=2)
810
Buffer data in a multiple-entry buffer at a data clock speed for each channel
820
Read buffered data at a system clock speed greater than the data clock speed for each channel
830
Determine if there is a danger of oversampling in any channel?
840
Y
N
Halt reading from all channels for one cycle of the system clock
850

Fig. 8

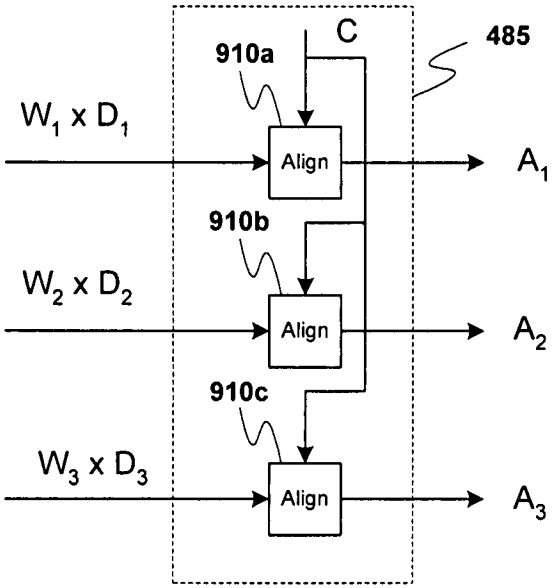
C
485
910a
$W_1 \times D_1$
Align
A_1
910b
$W_2 \times D_2$
Align
A_2
910c
$W_3 \times D_3$
Align
A_3

Fig. 9

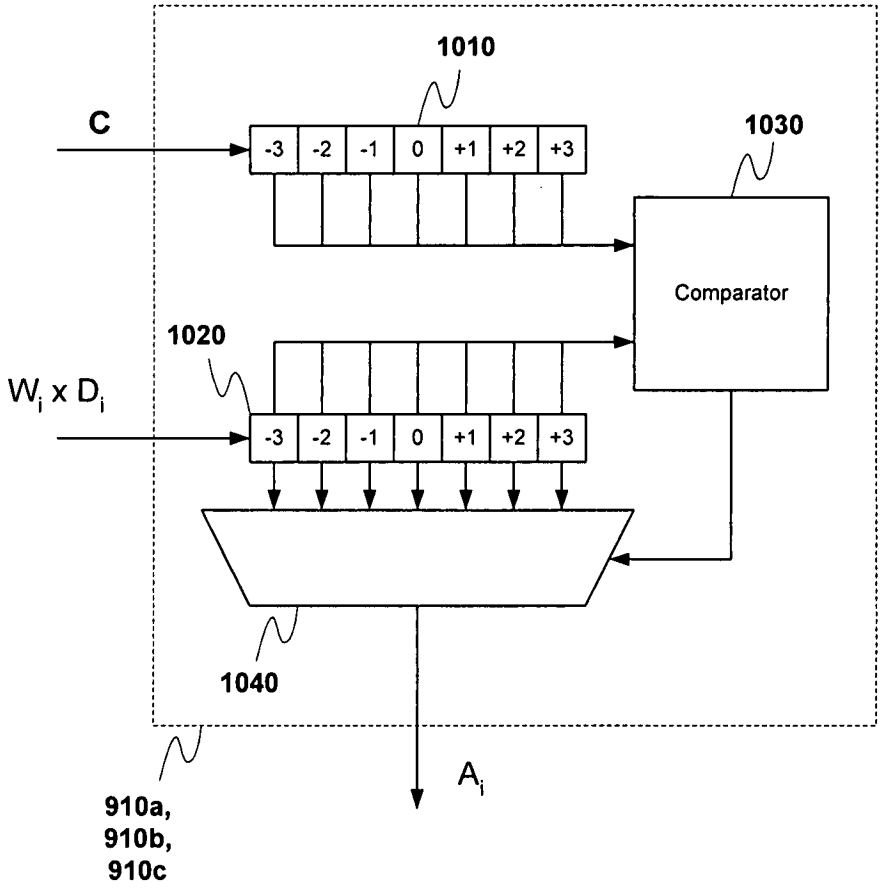
1010
C
-3
-2
-1
0
+1
+2
+3
1030
Comparator
1020
$W_i \times D_i$
-3
-2
-1
0
+1
+2
+3
1040
A_i
910a,
910b,
910c

Fig. 10